GF22: ONFI 4.1

Libraries

Name	Process	Form Factor
RGO_GF22_18V18_FDX_20C_ONFI_4_1	FDX	Staggered CUP

Summary

The ONFI 4.1 library provides the combo driver / receiver cells, the ODT / driver impedance calibration cell, and the voltage reference cell to support both single-ended and differential ONFI 4.1 signaling. This library also meets the requirements for ONFI 3.0 & Toggle 2.0 signaling. Also included is a full complement of power, spacer, and adapter cells to assemble a complete pad ring by abutment. An included rail splitter allows isolated ONFI domains to be placed in the same pad ring with other power domains while maintaining continuous VDD/VSS in the pad ring for robust ESD protection.

The ONFI 4.1 I/O library supports all impedance modes defined in the ONFI 4.1 specification and features fast and precise calibration, low power consumption, area-efficient design, and easy integration into the physical layer (PHY).

This 22nm library is available in a staggered CUP wire bond implementation with a flip chip option.

ESD Protection:

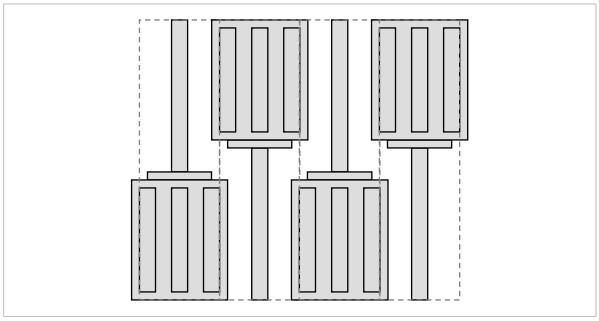
- JEDEC compliant
  - 2KV ESD Human Body Model (HBM)
  - 500 V ESD Charge Device Model (CDM)

Latch-up Immunity:

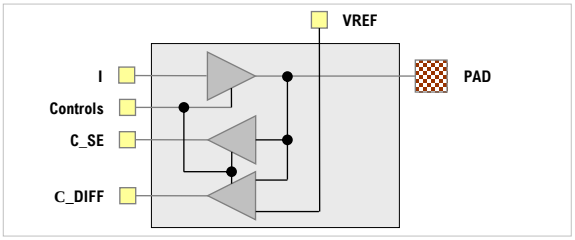
- JEDEC compliant
  - Tested to I-Test criteria of ± 100mA @ 125°C

Cell Size & Form Factor

Staggered (pad-limited) – TBDμm x TBDμm



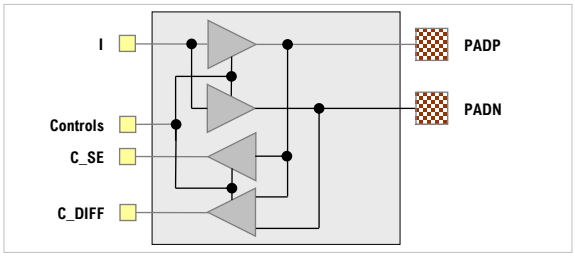
ONP_BI_SDS_1218V_SCB: Single-Ended Driver



ONFI Single-Ended Driver / Receiver Features:

- Driver – user-selectable on-die termination and programmable drive strength with ODT / Z_O calibration and programmable "off" state control.
  - ODT R_{tt} = 30Ω / 50Ω / 75Ω / 100Ω / 150Ω
  - Z_{OUT} = 18Ω / 25Ω / 35Ω / 50Ω
  - Off state – Z / pull-up / pull-down / bus keeper
- Receiver – single-ended and pseudo-differential outputs
- Powered by 1.2V / 1.8V I/O and 0.8V core supplies
- Maximum operating frequency – 400 MHz

ONP_CL_SDS_1218V_SCB: Differential Driver



ONFI Differential Clock Driver / Receiver Features:

- Driver – user-selectable on-die termination and programmable drive strength with ODT / Z_O calibration and programmable "off" state control.
  - ODT R_{tt} = 30Ω / 50Ω / 75Ω / 100Ω / 150Ω
  - Z_{OUT} = 18Ω / 25Ω / 35Ω / 50Ω
  - Off state – Z / pull-up / pull-down / bus keeper
- Receiver – single-ended and true differential outputs
- Powered by 1.2V / 1.8V I/O and 0.8V core supplies
- Maximum operating frequency – 400 MHz

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Recommended operating conditions

Symbol	Description		Min	Nom	Max	Units
V_{VDD}	Core supply voltage		0.72	0.80	0.88	V
T_J	Junction temperature		-40	25	125	°C
V_{PAD}	Voltage at PAD		-0.3V		V_{DVDD}+0.3V	V
V_{DVDD}	I/O supply voltage	NV-DDR	1.62	1.8	1.98	V
$V_{IH\ (DC)}$	Input High (DC)	NV-DDR	0.7 * V_{DVDD}		V_{DVDD} + 0.3	V
$V_{IL\ (DC)}$	Input Low (DC)	NV-DDR	V_{DVSS} - 0.3		0.3 * V_{DVDD}	V
$V_{IH\ (AC)}$	Input High (AC)	NV-DDR	0.8 * V_{DVDD}		V_{DVDD} + 0.3	V
$V_{IL\ (AC)}$	Input Low (AC)	NV-DDR	V_{DVSS} - 0.3		0.2 * V_{DVDD}	V
V_{DVDD}	I/O supply voltage	NV-DDR2	1.62	1.8	1.98	V
$V_{IH\ (DC)}$	Input High (DC)	NV-DDR2	V_{REF} +.125		V_{DVDD} + 0.3	V
$V_{IL\ (DC)}$	Input Low (DC)	NV-DDR2	V_{DVSS} - 0.3		V_{REF} -.125	V
$V_{IH\ (AC)}$	Input High (AC)	NV-DDR2	V_{REF} +.250			V
$V_{IL\ (AC)}$	Input Low (AC)	NV-DDR2			V_{REF} -.125	V
V_{DVDD}	I/O supply voltage	NV-DDR3	1.14	1.2	1.26	V
$V_{IH\ (DC)}$	Input High (DC)	NV-DDR3	V_{REF} +.100		V_{DVDD} + 0.3	V
$V_{IL\ (DC)}$	Input Low (DC)	NV-DDR3	V_{DVSS} - 0.3		V_{REF} -.100	V
$V_{IH\ (AC)}$	Input High (AC)	NV-DDR3	V_{REF} +.150			V
$V_{IL\ (AC)}$	Input Low (AC)	NV-DDR3			V_{REF} -.150	V

Characterization Corners

Nominal VDD	Model	VDD	DVDD	Temp
0.8V	FF	+10%	See table below for DVDD voltage ranges.	-40°C
	FF	+10%		0°C
	TT	nominal		25°C
	TT	nominal		85°C
	SS	-10%		-40°C
	SS	-10%		125°C

Library Characterization DVDD Voltage Ranges

Nominal DVDD		FF	TT	SS	Units
1.8	NV-DDR & NV-DDR2	1.95	1.8V	1.7	V
1.2	NV-DDR3	1.26	1.2	1.14	V

Cell summary

Name	Description
ONP_BI_SDS_1218V_SCB *	ONFI Single-Ended Driver/Receiver
ONP_CL_SDS_1218V_SCB *	ONFI Differential Clock Driver/Receiver
ONP_SP_CAL_1218V *	Calibration cell
ONP_RE_000_1218V *	Voltage Reference (VREF).
PVP_VD_PDO_1218V *	I/O V_{DD} (DVDD) with POC
PVP_VD_RDO_1218V *	I/O V_{DD} (DVDD)
PVP_VS_RDO_1218V *	I/O V_{SS} (DVSS)
PVP_VS_DRC_1218V *	I/O V_{SS} (DVSS is shorted to VSS)
PVP_VD_RCD_0918V *	Core V_{DD} (VDD)
PVP_VS_RCD_0918V *	Core V_{SS} (VSS)
PVP_VS_DRC_0918V *	Core V_{SS} (DVSS is shorted to VSS)
SVP_CO_000_1218V	Corner cell – rail splitter
SVP_CO_001_1218V	Corner cell - continous
SVP_SP_001_1218V	1µm spacer cell
SVP_SP_005_1218V *	5µm spacer cell
SVP_SP_020_1218V *	20µm spacer cell
SPP_RS_005_1218V	Rail splitter cell
SPP_SP_CAP_1218V	Core decoupling cap cell

* Vertical-only and horizontal-only orientations

Staggered CUP Cells	
CUP_GF22_TBD_IN	TBD X TBD Inner
CUP_GF22_TBD_OUT	TBD X TBD Outer
CUP_GF22_FC	Flip chip with top metal port
CUP_GF22_FC_NRV	Flip chip without RV vias

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